深圳市硅传科技有限公司

Tel:086-0755-33592127
Fax:086-0755-36862612
Web:www.silicontra.com

CC2500TR2.4

2.4GHz FSK/MSK/ASK/OOK 收发模块

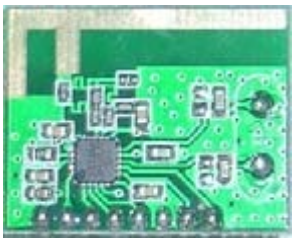
Description

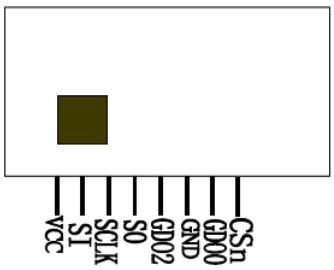
CC2500 is a FSK/ASK/OOK/MSK Transceiver module.It provides extensive hardware support for packet handling,data buffering,burst transmissions ,clear channel assessment, link quality indication and wake on radio.It 's data stream can be manchester coded by the modulator and decoded by the demodulator .It has a high performance and easily to design your product.It can be used in 2400-2483.5MHz ISM/SRD band systems,Consumer Electronics, Wireless game controllers,Wireless audio and others wireless systems.

we support the frequency have 2400-2483.5MHz ISM Band modules now.

一般描述

CC2500 是集 FSK/ASK/OOK/MSK.调制方式于一体的收发模块。它提供扩展 硬件支持实现信息包处理、数据缓冲、群发射、空闲信道评估、链接质量指 示和无线唤醒，可以采用曼彻斯特编码进行调制解调它的数据流。性能优越 并且易于应用到你的产品设计中，它可以应用在 2400-2483.5MHz ISM/SRD 频段的系统中，比如消费类电子产品、无线游戏控制器、无线音频传输等等。 我们目前支持 2400-2483.5MHz 范围的 ISM 频段的模块





Features

Low current consumption.
Easy for application.
Efficient SPI interface
Operating temperature range
Operating voltage
Available frequency at
Programmable output power and hi sensitivity

基本特征

●低电流损耗
●方便投入应用
●高效的串行编程接口
●工作温度范围： －40℃～＋85℃
●工作电压：1.8~ 3.6 Volts.
●有效频率：2.4-2.483GHz
●灵敏度高、输出功率可编程

Applications

2400-2483.5MHz ISM/SRD band systems
Consumer Electronics
Wireless game controllers
Wireless audio
Wireless keyboard and mouse

应用领域

●2400-2483.5MHz ISM/SRD 频带系统
●消费类电子产品
●无线游戏控制器
●无线音频传输
●无线键盘、鼠标

Pin Descriptions 管脚描述

Pin No	Pin Name	Pin Type	Description 一般描述
1	VCC	Power	1.8V-3.6V power 1.8~3.6 电源
2	SI	Digital Input	Serial configuration interface, data input 串行配置接口，数据输入
3	SCLK	Digital Input	Serial configuration interface, clock input 串行配置接口，时钟输入
4	SO	Digital Output	Serial configuration interface, data output. 串行配置接口，数据输出 Optional general output pin when CSn is high CSn 高电平时，可选通用输出
5	GDO2	Digital Output	Digital output pin for general use: 通用数字信号输出： • Test signals • 测试信号 • FIFO status signals • 先进先出堆栈状态信号 • Clear Channel Indicator • 空闲信道指示 • Clock output, down-divided from XOSC • 时钟输出，从 XOSC 分频 • Serial output RX data • 串行输出接收数据
6	GND	Ground	GND 地
7	GDO0	Digital I/O	Digital output pin for general use: 通用数字信号输出： • Test signals • 测试信号 • FIFO status signals • 先进先出堆栈状态信号 • Clear Channel Indicator • 空闲信道指示 • Clock output, down-divided from XOSC • 时钟输出，从 XOSC 分频 • Serial output RX data • 串行输出接收数据 • Serial input TX data • 串行输入发射数据
8	CSn	Digital Input	Serial configuration interface, chip select 串行配置接口，芯片选择

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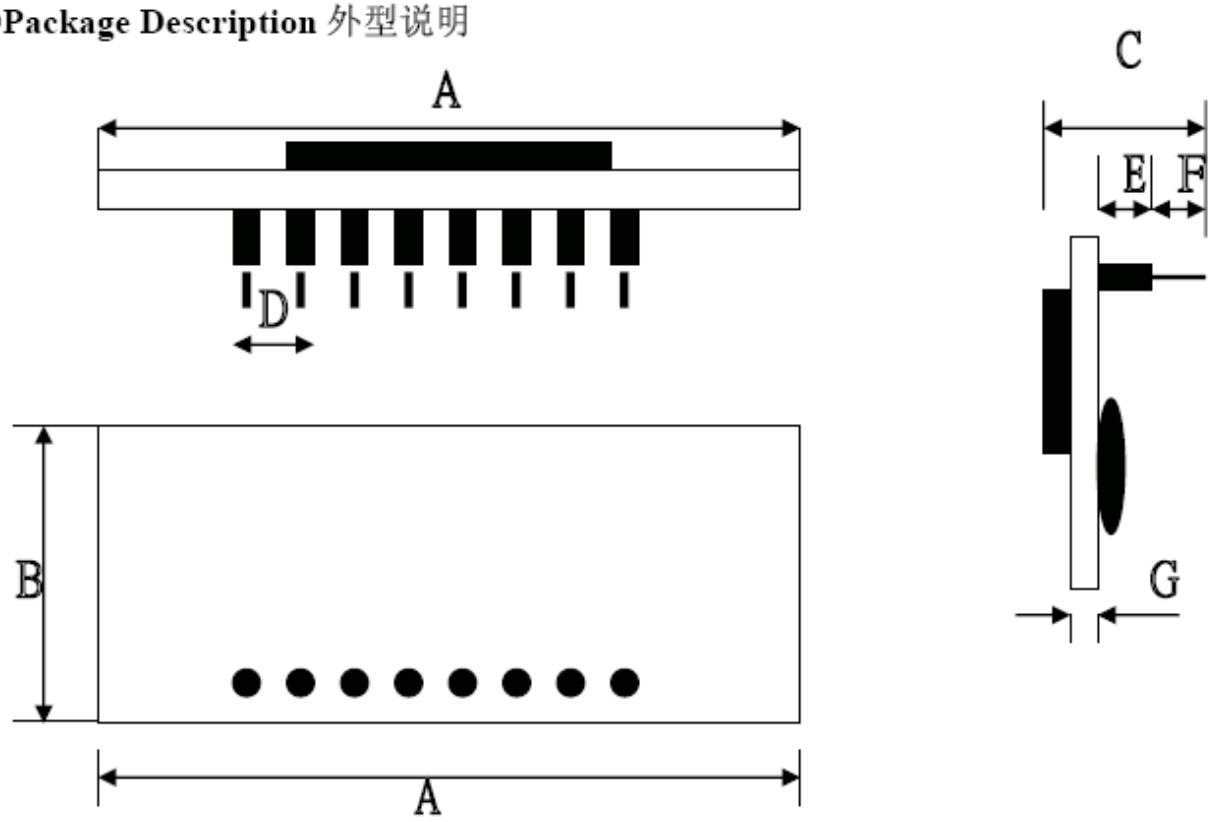
Absolute Maximum Ratings 极限参数

Parameter（参数）	Rating（额定值）	Units（单位）
Supply Voltage（工作电压）		
Operating Temperature（工作温度）		℃

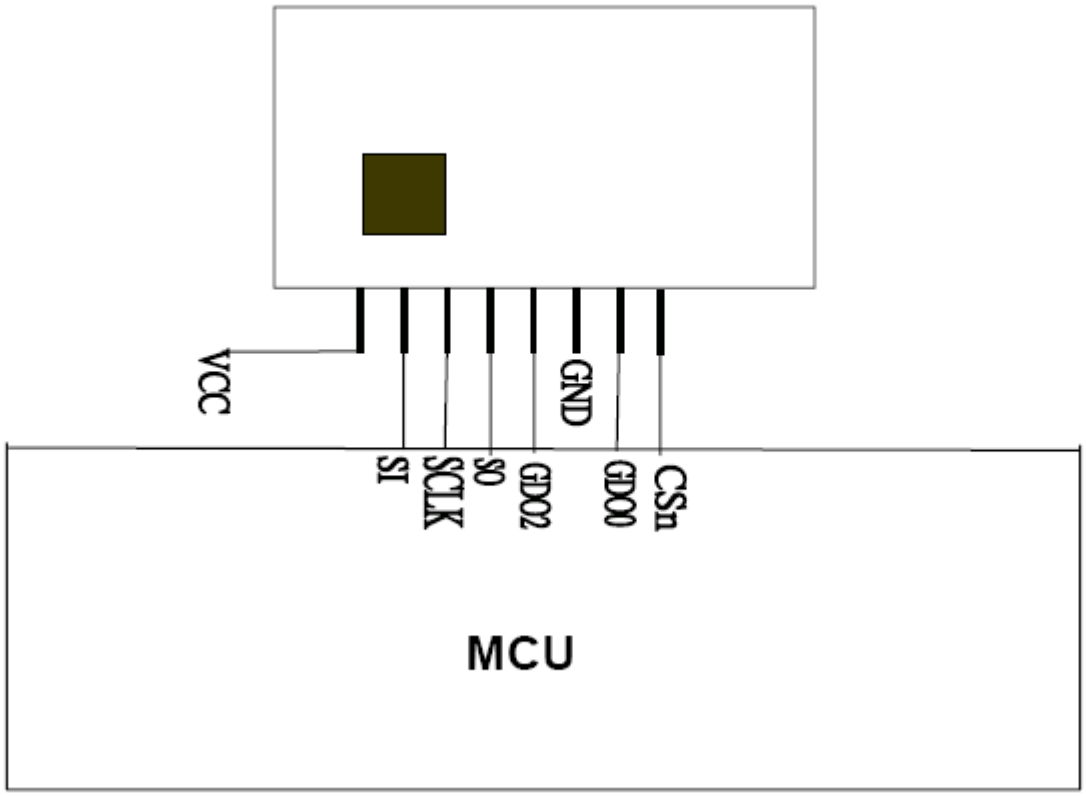
Package Description 外型说明

▪Package Description 外型说明



Name 名称	Dimension 尺寸	Name 名称	Dimension 尺寸
A	24mm+-0.5mm	E	2.17mm
B	19mm+-0.5mm	F	3.6mm+-0.2mm
C	8.8mm (Max)	G	1.0mm
D	2.0mm		

Application Circuit 典型应用电路



Module Program 模块编程

1. Configuration Software 配置软件

CC2500 can be configured using the SmartRF® Studio software, available for download from http://www.chipcon.com. The SmartRF® Studio software is highly recommended for obtaining optimum register settings, and for evaluating performance and functionality.

可以利用 SmartRF® Studio 软件对 CC2500 进行配置，该软件可以从网站 http://www.chipcon.com 下载。SmartRF® Studio 是被高度推荐用来获得最合适的寄存 器配置，和用来评估模块性能和功能的软件。

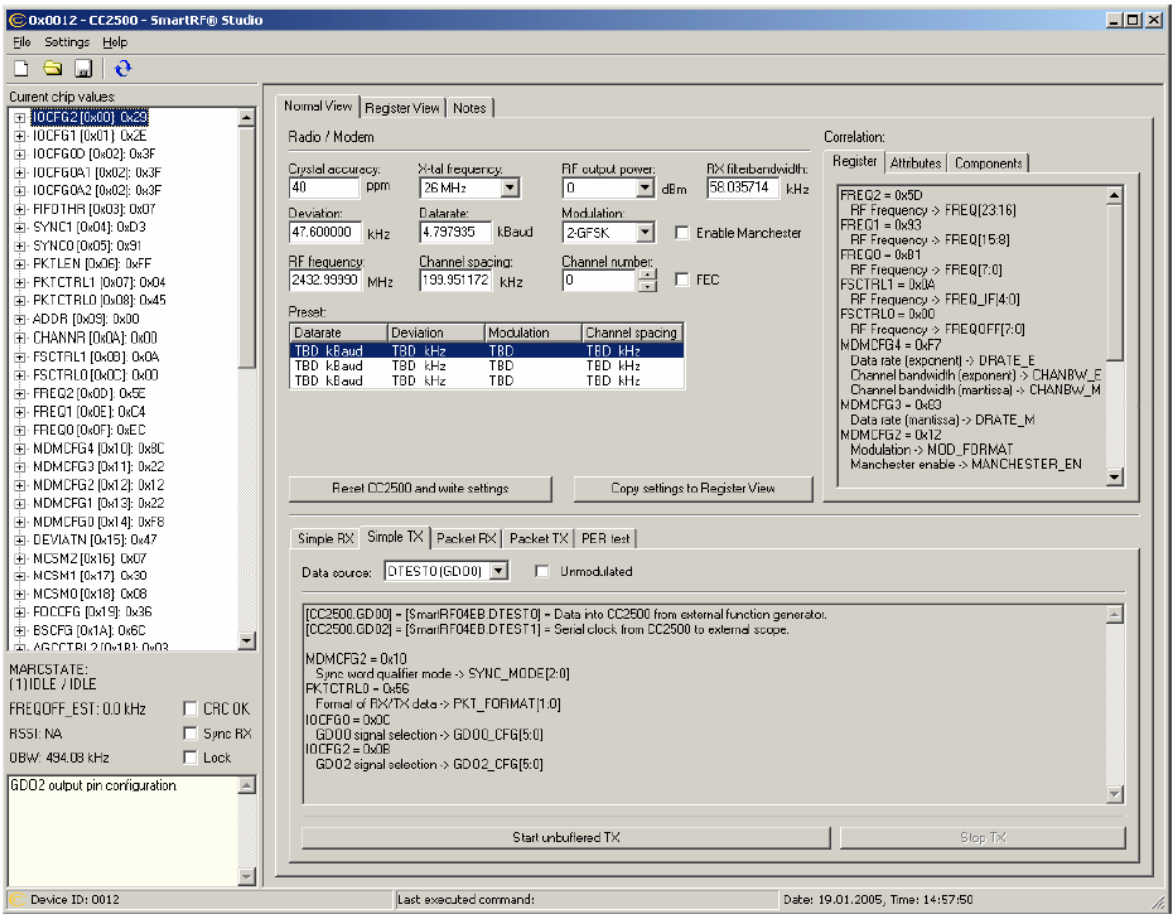


Figure 5: SmartRF® Studio user interface

2. 4-wire Serial Configuration and Data Interface

CC2500 is configured via a simple 4-wire SPI compatible interface (SI, SO, SCLK and CSn) where CC2500 is the slave. This interface is also used to read and write buffered data. All address and data transfer on the SPI interface is done most significant bit first

CC2500 是通过一个简单的 4 线 SPI 兼容接口（SI，SO，SCLK，CSn）来配置，这时 CC2500 工作于 slave 模式。该接口也用于读写缓冲器的数据。所有的地址和数据在 SPI 口的传送 都是从最高位开始的。

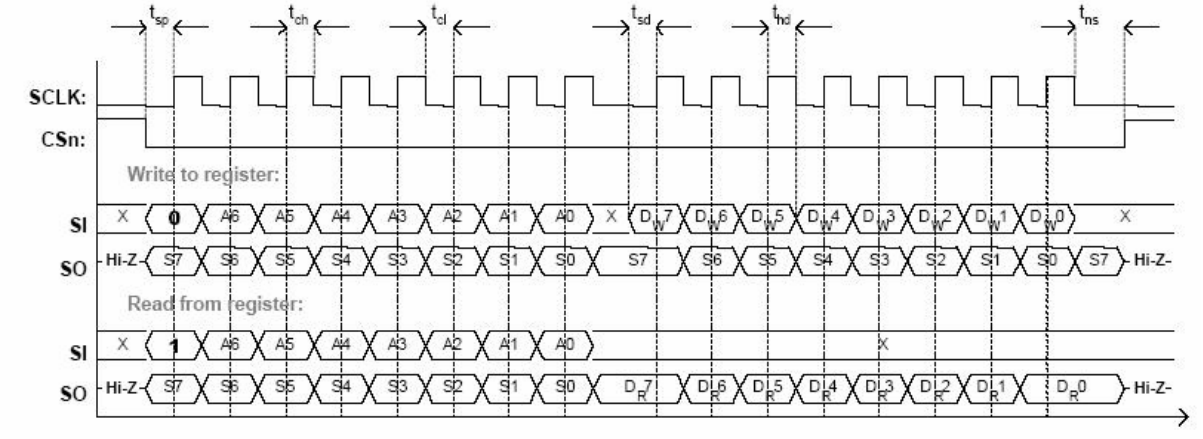


Figure 6: Configuration registers write and read operations

Register access types 寄存器访问类型如下图：

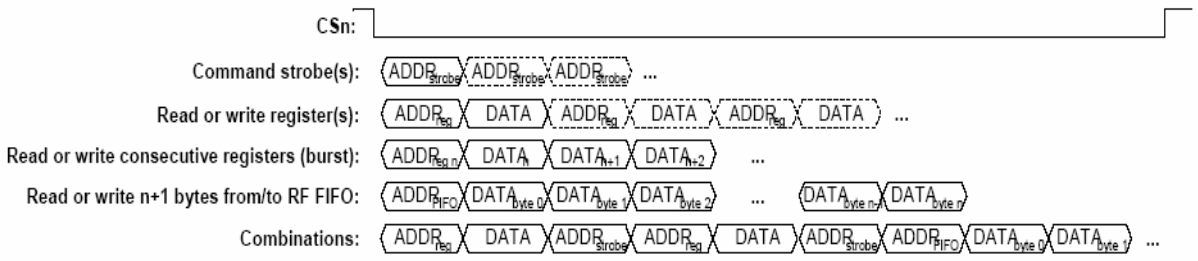


Figure 7: Register access types

3．Packet Format 数据包格式

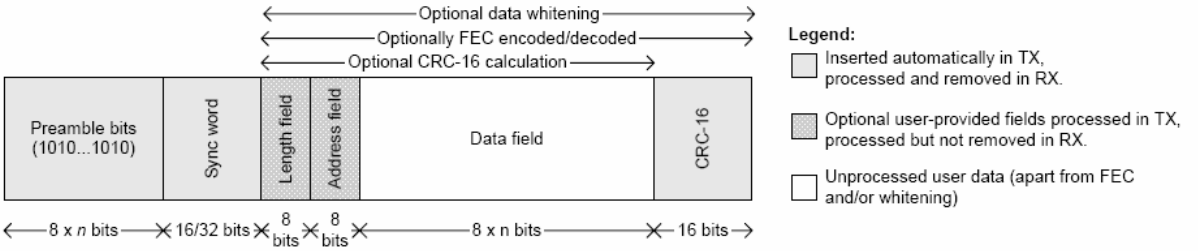


Figure 8: Packet Format

4．Power on start-up sequence 上电启动顺序

The power-up sequence is as follows (see Figure 11):

- Set SCLK=1 and SI=0, to avoid potential problems with pin control mode .
- Strobe CSn low / high.
- Hold CSn high for at least 40µs.
- Pull CSn low and wait for SO to go low (CHIP_RDYn).
- Issue the SRES strobe.
- When SO goes low again, reset is complete and the chip is in the IDLE state.

power-up 的操作顺序如下：

.设置 SCLK=1 和 SI=0，以避免 PIN 脚控制模式造成的潜在问题。
.设置 CSn 为低然后再拉高。
.保持 CSn 为高至少 40us。
.将 CSn 拉低等待 SO 变低（CHIP_RDYn）.
.发送 SRES 命令.
.当 SO 再次变低后,复位工作就完成了,IC 处于 IDLE 状态.

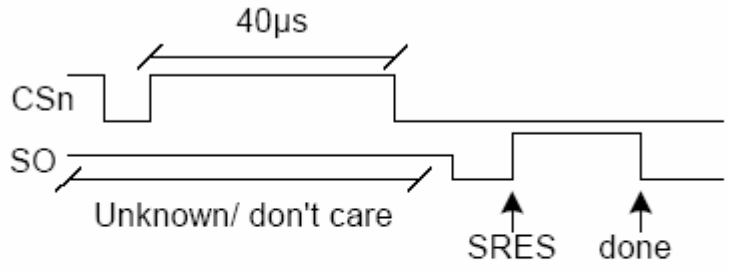


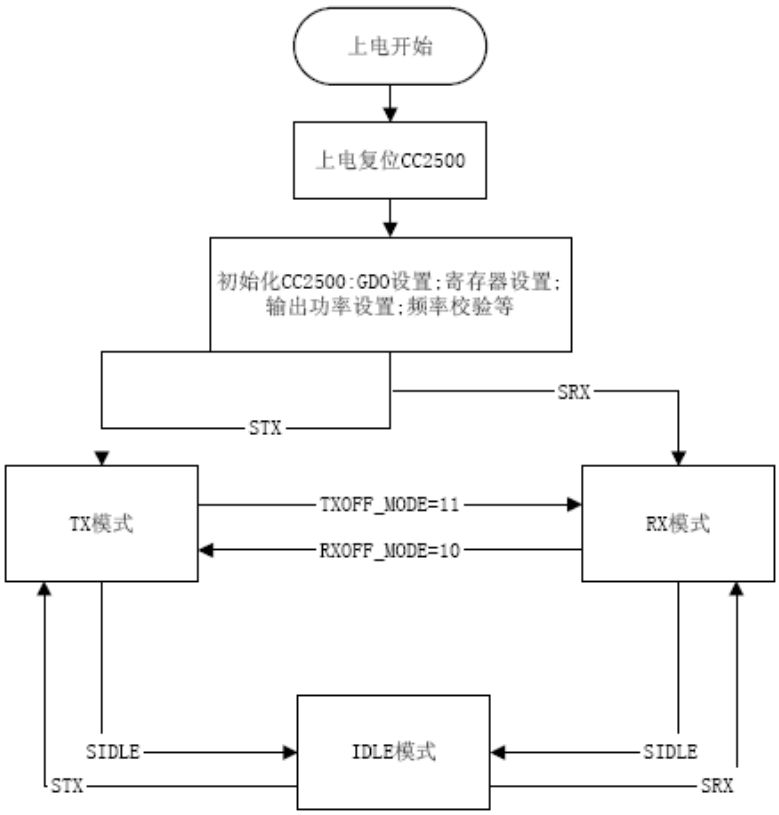
Figure 11: Power-up with SRES

5. Output power levels 输出功率表：

Output power [dBm]	Setting	Current consumption, typ. [mA]
(–55 or less)	0x00	8.9
–30	0x44	10.1
–28	0x41	10.0
–26	0x4C	11.7
–24	0x53	11.1
–22	0x83	10.9
–20	0x46	10.5
–18	0x4A	11.7
–16	0x86	11.0
–14	0x66	12.9
–12	0xC6	11.5
–10	0x69	14.1
–8	0x99	13.6
–6	0x7F	15.4
–4	0xAA	16.7
–2	0xBF	18.5
0	0xFB	21.6
1	0xFF	21.9

Table 22: Optimum PATABLE settings for various output power levels (subject to changes)

6．Reference flow chart 参考流程图：



流程图